MEMORY DEVICE AND METHOD OF

STORING FAIL ADDRESSES OF A MEMORY CELL

ABSTRACT

The embodiments of the present invention are directed to a self-repair schema for memory chips, using a sortable fail-count / fail-address register. The embodiments of the present invention utilize the available redundancy efficiently by scanning the memory array to locate the n elements (WLs or CSLs) with the highest number of defects. A circuit preferably comprises one or more comparators to compare a fail count of an address in an input register with at least one fail count stored in the sortable fail-count / fail-address register. The embodiments of the present invention can be used for an on-chip redundancy calculation and can handle a two dimensional (i.e. row and column) redundancy.